Ramgarhia Polytechnic College, Phagwara

Computer Science Engineering Department

Head of Department:	Er. Poonam Rana
Name of the Faculty:	Er. Simranjit Singh Kahlon
Discipline:	CSE
Semester:	3rd
Subject:	Digital Electronics
Lesson Plan Duration:	16 Weeks

RATIONALE

This course has been designed to make the students know about the fundamental principles of digital electronics and gain familiarity with the available IC chips. This subject aims to give a background in the broad field of digital systems design and microprocessors.

LEARNING OUTCOMES

After undergoing the subject, student will be able to:

CO1. Verify and interpret truth tables for all logic gates.
CO2. Realize all logic functions with NAND and NOR gates.
CO3. Design half adder and full adder circuit.
CO4. Demonstrate and design 4-bit adder, 2's complement subtractor.
CO5. Verify and interpret truth tables for all flip flops.
CO6. Verify and interpret truth tables of multiplexer, de-multiplexer, encoder and decoder ICs.
CO7. Design a four bit ring counter and verify its operation.
CO8. Design 4-bit SISO, PISO, SIPO, PIPO shift registers.

PO ⇨ / CO ⇩	PO1	PO2	PO3	PO4	PO5	PO6	PO7
CO1							
CO2							
CO3							
CO4							
CO5							
CO6							
CO7							
CO8							

Syllabus

Units	Details	Hours
1.	Introduction a) Distinction between analog and digital signal. b) Applications and advantages of digital signals	(02 hrs)
2.	Number System a) Binary, octal and hexadecimal number system: conversion from decimal and hexadecimal to binary and vice-versa. b) Binary addition, subtraction, multiplication and division including binary points. Sign magnitude method of representation, 1's and 2's complement method of addition/subtraction, floating point representation	(04 hrs)
3.	Codes and Parity a) Concept of code, weighted and non-weighted codes, examples of BCD, excess-3 and Gray code. b) Concept of parity, single and double parity and error detection and correction (Hamming code) c) Alpha numeric codes: ASCII, EBCDIC and Unicode.	(04 hrs)
4.	Logic Gates and Families a) Concept of negative and positive logic b) Definition, symbols and truth tables of gates. Construction of NOT, AND and OR gates from NAND and NOR gates (universal gates). (c) Introduction to TTL and CMOS logic families and their sub classification	(07 hrs)
5.	Logic Simplification a) Postulates of Boolean algebra, De Morgan's Theorems. Various identities. Formulation of truth table and Boolean equation for simple problem. Implementation of Boolean (logic) equation with gates b) Karnaugh map (upto 4 variables) and simple application in developing combinational logic circuits	(06 hrs)
6.	Arithmetic circuits a) Half adder and Full adder circuit, design and implementation. b) Half and Full subtracter circuit, design and implementation. c) 4 bit adder/subtracter. d) Adder and Subtractor IC (7484) e) 2-bit comparator	(06 hrs)
7.	Decoders, Multiplexers and De-Multiplexers (06 hrs) a) Basic functions and block diagram of Encoders and decoders. b) Basic functions and block diagram of Multiplexers and De-Multiplexers. Different types and ICs. c) Four bit decoder circuits for 7 segment display and decoder/driver ICs.	(06 hrs)

8.	Latches and flip flops a) Concept and types of latch with their working and applications b) Operation using waveforms and truth tables of RS, T, D, JK and Master/Slave JK flip flops. c) Difference between a latch and a flip flop d) Flip flop ICs	(06 hrs)
9.	Shift Register Introduction and basic concepts including shift left and shift right. a) Serial in parallel out, serial in serial out, parallel in serial out, parallel in parallel out. b) Universal shift register c) Buffer register, Tristate Buffer register d) IC 7495	(07 hrs)
10.	Counters a) Introduction to Asynchronous and Synchronous counters b) Binary up/down counters (upto MOD-8) c) Decade counter. d) Pre settable and programmable counters e) Ring counter with timing diagram f) Counter ICs	(08 hrs)
11.	Analog to Digital and Digital to Analog Converters a) Working principle of A/D and D/A converters b) Detail study of : ➢ Binary Weighted D/A converter ➢ R/2R ladder D/A converter ❖ Brief idea about different techniques of A/D conversion and study of : ➢ Stair step Ramp A/D converter ➢ Dual Slope A/D converter ➢ Successive Approximation A/D Converter ❖ Performance characteristics of A/D and D/A converter. ❖ Applications of A/D and D/A converter.	(08 hrs)

Reference Books:

1. Digital Electronics and Applications by Malvino Leach, Tata McGraw Hill Education Pvt Ltd, New Delhi.
2. Digital Logic Designs by Morris Mano, Prentice Hall of India, New Delhi

3. Digital Circuits and Design by DP Kothari and JS Dhillon, Pearson Publication, New Delhi
4. Digital Electronics by Soumitra Kumar Mandal, Tata McGraw Hill Education Pvt Ltd.
5. Digital Electronics by Tokheim, Tata McGraw Hill Education Pvt Ltd.
6. Digital Fundamentals by Thomas Floyds, Universal Book Stall
7. Digital Electronics by RP Jain, Tata McGraw Hill Education Pvt Ltd, New Delhi
8. Digital Electronics by KS Jamwal, Dhanpat Rai and Co., New Delhi

Delivery/Instructional Methodologies

Sr.No.	Description
1.	Chalk and Talk
2.	PowerPoint Presentation

Assessment Methodologies

Sr. No.	Description	Type
1.	Student Assignment	Direct
2.	Test	Direct
3.	Board Examination	Direct
4.	Student Feedback	Direct

Gaps in the syllabus - to meet industry/profession requirements

S.NO.	DESCRIPTION	PROPOSED ACTIONS	PO MAPPING
	N/A	N/A	N/A

Topics beyond syllabus/advanced topics

Units	Details	Hours
N/A	N/A	N/A

Web Source References

Sr. No.	URL
1.	https://nptel.ac.in/

Lesson Plan

Week	Theory		Practical	
	Lecture Day		Practical Day	
1st	1st	Distinction between analog and digital signals	1.	Verification and interpretation of truth tables for AND, OR, NOT NAND, NOR and Exclusive OR (EXOR) and Exclusive NOR(EXNOR) gates
	2nd	Applications and advantages of digital signals		
	3rd	Binary,Octaland hexadecimal number system: conversion from decimal and hexadecimal to binary		
	4th	Vice- versa conversions.		
2nd	5th	Binary addition, subtraction,division	2.	Realisation of logic functions with the help of NAND or NOR gates
	6th	1's and 2's complement method of addition/ subtraction, floating point		

		representation.		
	7th	Concept of code, weighted and non weighted codes,BCD, EXCESS-3 AND GRAY CODE		
	8th	Concept of parity,single and double parity and error detection and correction(Hamming Code)		
3rd	9th		3.	Design of a NOR gate latch and verification of its operation
	10th	Alpha numeric codes ASCII,EBCDIC		
	11th	Concept of negative and positive logic		
	12th	Definition , Symbol and truth tables of logic gates. NOT, AND AND OR gate from NAND and NOR gates		
4th	13th		4.	- To design a half adder using XOR and NAND gates and verification of its operation - Construction of a full adder circuit using XOR and NAND gates and verify its operation
	14th			
	15th			
	16th	Introduction to TTL and CMOS logic families and their sub classifications.		
5th	17th		5.	To design 4 bit adder, 2's complement subtractor circuit using an 4 bit adder IC and an XOR IC and verify the operation of the circuit.
	18th	Postulates of Boolean algebra, De morgan's theorems		
	19th	Various identities formulation of truth table and Boolean equation for simple problem.		
	20th			
6th	21st	Implementation of Boolean equations with gates	6.	To design a NOR Gate Latch and verification of its operation

	22nd	Karnaugh map and simple application in developing combinational logic circuits		
	23rd			
	24th	**1st Sessional Test (Tentative)**		
7th	25th	Half adder and full adder circuit design and implementation	7.	Verification of truth table for positive edge triggered, negative edge triggered, level triggered IC flip-flops (At least one IC each of D latch , D flip-flop, JK flip-flops).
	26th	Half and full subtractor circuit design and implementation		
	27th	4 bit adder and subtractor		
	28th	Adder and subtractorIC(7484)		
8th	29th	2-bit comparator	8.	Verification of truth table for encoder and decoder ICs, Mux and DeMux
	30th	**REVISION**		
	31st	Basic function and block diagram of encoders and decoders		
	32nd			
9th	33rd	Basic functions and block diagram o multiplexers and demultiplexers. Different types of IC's	9.	To design a 4 bit SISO, SIPO, PISO, PIPO shift registers using JK/D flip flops and verification of their operation.
	34th			
	35th	Four bit decoder circuits for seven segment display and decoder/driver Ic's		
	36th			
10th	37th	Concept and types of latch with their working and applications	10.	To design a 4 bit SISO, SIPO, PISO, PIPO shift registers using JK/D flip flops and verification of their operation.

10th	38th	Operation using waveforms and truth tables of RS,T,D,JK AND MASTER /SLAVE JK Flip Flops		
	39th			
	40th			
11th	41st	Difference between latch and a flip flop	11.	To design a 4 bit ring counter and verify its operation.
	42nd	Flip flop Ic's		
	43rd			
	44th	SISO,SIPO shift resgisters		
12th	45th	**PTM**	12.	**REVISION/VIVA VOICE**
	46th	**2nd Sessional Test (Tentative)**		
	47th	PISO,PIPO shift resgiters, Universal shift register		
	48th	Buffer register, Tristate Buffer register		
13th	49th		13.	Asynchronous Counter ICs Verification of truth table for any one universal shift register IC Use of IC 7490 or equivalent TTL (a) divide by 2 (b) divide by 10 Counter
	50th	IC7495		
	51st	Introduction to Asynchronous and synchronous counters		
	52nd	Binary up/down counters		

14th	53rd	Decade counters	14	Use of IC 7493 or equivalent TTL (a) divide by 2 (b) divide by 8 (c) divide by 16 counter
	54th	Pre settable and programmable counters		
	55th	Ring counter with timing diagram		
	56th	Counters IC'S		
15th	57th	Working principle of A/D and D/a converters	15.	**Practical performance TEST**
	58th	Binary weighted D/A converter and R/2R ladder D/A converter		
	59th	Stair step ramp A/D converter,dual slope A/D converter,successive approximation A/D converter		
	60th			
16th	61st	Performance characteristics of A/D and D/A converters.	16.	**Practical performance TEST**
	62nd	Applications of A/D and D/A converters		
	63rd	**PTM**		
	64th	**3rd Sessional Test (Tentative)**		